DATA SHEET

74ABT544

Octal latched transceiver with dual enable, inverting (3-State)

Product data
Supersedes data of 1993 Jun 01

2002 Nov 18

Philips
Semiconductors

PHILIPS

Octal latched transceiver with dual enable, inverting (3-State)

74ABT544

FEATURES

- Combines 74ABT640 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64 mA/–32 mA
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT544 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT544 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64 mA.

FUNCTIONAL DESCRIPTION

The 74ABT544 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are LOW, the A-to-B path is transparent. A subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both LOW, the 3-State B output buffers are active and invert the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

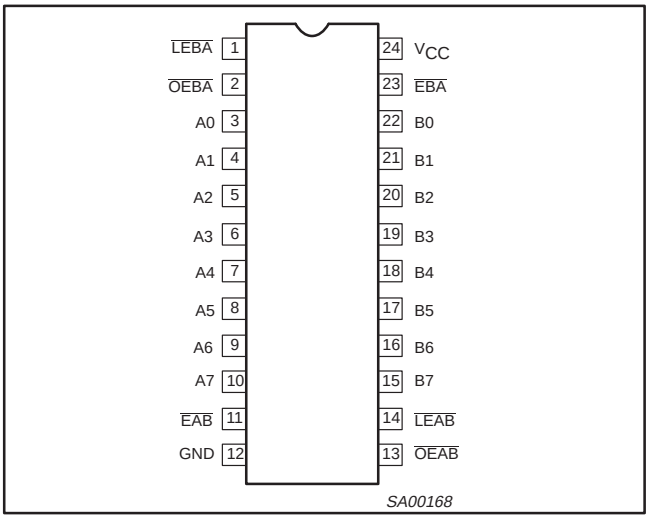
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50 pF; V_{CC} = 5 V	3.9	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0 V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5 V	110	μA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	TEMPERATURE RANGE	DWG NUMBER
74ABT544N	DIP24: 24-pin plastic dual in-line package	–40 °C to +85 °C	SOT222-1
74ABT544D	SO24: 24-pin plastic small outline package	–40 °C to +85 °C	SOT137-1
74ABT544DB	SSOP24: 24-pin plastic shrink small outline package; Type II	–40 °C to +85 °C	SOT340-1
74ABT544PW	TSSOP24: 24-pin thin shrink small outline package; Type I	–40 °C to +85 °C	SOT355-1

PIN CONFIGURATION



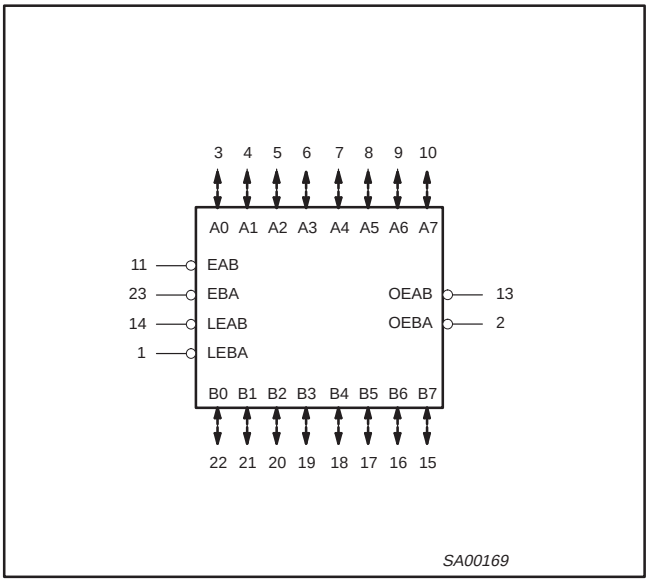
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A-to-B / B-to-A Latch Enable input (active-LOW)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A-to-B / B-to-A Enable input (active-LOW)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A-to-B / B-to-A Output Enable input (active-LOW)
3, 4, 5, 6, 7, 8, 9, 10	A0 – A7	Port A, 3-State outputs
22, 21, 20, 19, 18, 17, 16, 15	B0 – B7	Port B, 3-State outputs
12	GND	Ground (0 V)
24	V_{CC}	Positive supply voltage

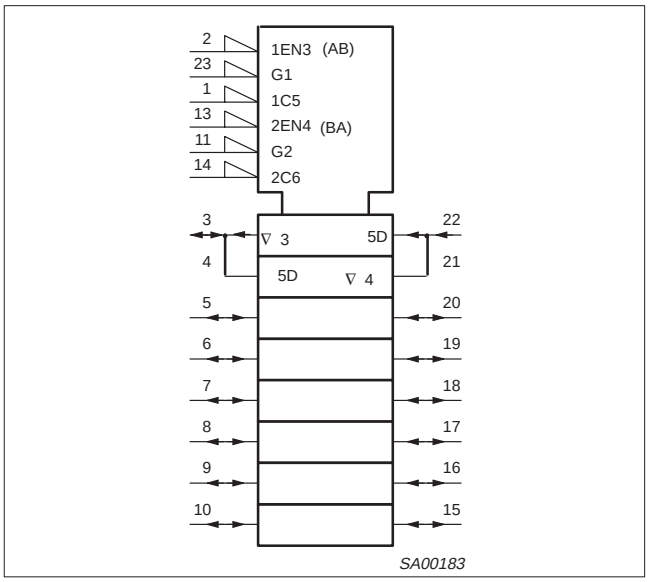
Octal latched transceiver with dual enable, inverting (3-State)

74ABT544

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

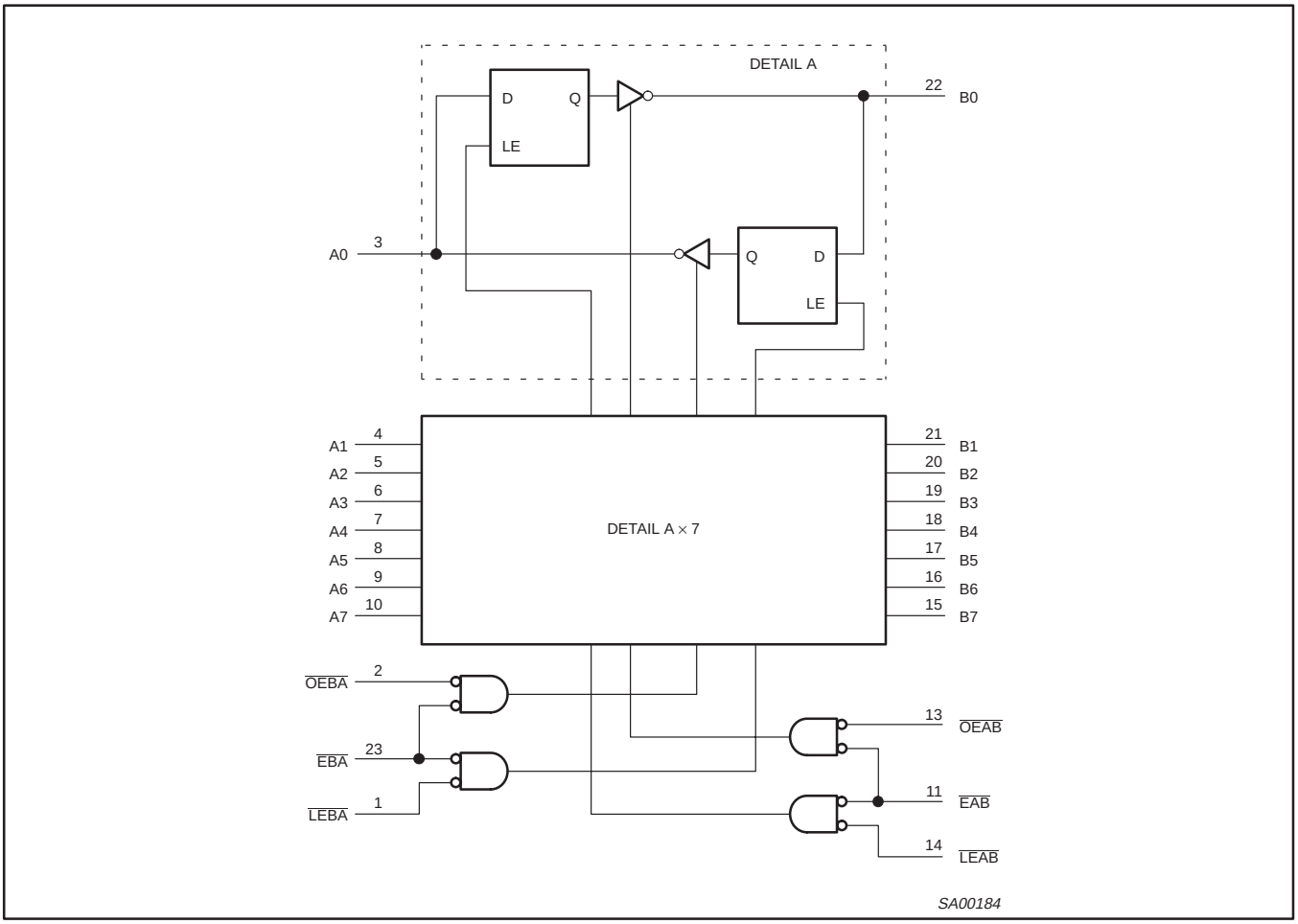


FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	An or Bn	An or Bn	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	L H	Latch + Display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition
NC= No change
Z = High impedance or "OFF" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	–50	mA
V_{OUT}	DC output voltage[3]	output in OFF or HIGH state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in LOW state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0	–	V
V_{IL}	Low-level Input voltage	–	0.8	V
I_{OH}	High-level output current	–	–32	mA
I_{OL}	Low-level output current	–	64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25 °C			T_{amb} = –40 °C to +85 °C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5 V; I_{IK} = –18 mA	–	–0.9	–1.2	–	–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	2.5	3.2	–	2.5	–	V
			V_{CC} = 5.0 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	3.0	3.7	–	3.0	–	V
			V_{CC} = 4.5 V; I_{OH} = –32 mA; V_I = V_{IL} or V_{IH}	2.0	2.3	–	2.0	–	V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}	–	0.42	0.55	–	0.55	V
V_{RST}	Power-up output low voltage[3]		V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	–	0.13	0.55	–	0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5 V; V_I = GND or 5.5 V	–	±0.01	±1.0	–	±1.0	µA
		Data pins	V_{CC} = 5.5 V; V_I = GND or 5.5 V	–	±5	±100	–	±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0 V; V_I or $V_O \leq$ 4.5 V	–	±5.0	±100	–	±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]		V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{OE} = Don't care	–	±5.0	±50	–	±50	µA
$I_{IH} + I_{OZH}$	3-State output HIGH current		V_{CC} = 5.5 V; V_O = 2.7 V; V_I = V_{IL} or V_{IH}	–	5.0	50	–	50	µA
$I_{IL} + I_{OZL}$	3-State output LOW current		V_{CC} = 5.5 V; V_O = 0.5 V; V_I = V_{IL} or V_{IH}	–	–5.0	–50	–	–50	µA
I_{CEX}	Output HIGH leakage current		V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}	–	5.0	50	–	50	µA
I_O	Output current[1]		V_{CC} = 5.5 V; V_O = 2.5 V	–50	–65	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5 V; Outputs HIGH; V_I = GND or V_{CC}	–	110	250	–	250	µA
I_{CCL}			V_{CC} = 5.5 V; Outputs LOW; V_I = GND or V_{CC}	–	20	30	–	30	mA
I_{CCZ}			V_{CC} = 5.5 V; Outputs 3-State; V_I = GND or V_{CC}	–	110	250	–	250	µA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND; V_{CC} = 5.5 V	–	0.3	1.5	–	1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. For valid test results, data must not be loaded into the flip–flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition of 10 msec. From V_{CC} = 2.1 V to V_{CC} = 5V ± 10%, a transition time of up to 100 µsec is permitted.

AC CHARACTERISTICS

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25 °C, V_{CC} = +5.0 V			T_{amb} = –40 °C to +85 °C, V_{CC} = +5.0 V ±0.5 V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	1	1.1 1.4	3.6 3.9	5.1 5.4	1.1 1.4	6.1 6.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	1, 2	1.6 2.1	4.1 4.6	5.6 6.1	1.6 2.1	6.6 7.1	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	1.4 2.5	3.9 5.0	5.4 6.5	1.4 2.5	6.4 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	2.5 1.0	5.9 5.5	7.4 7.0	3.4 3.0	8.4 8.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	4 5	1.4 2.5	3.9 5.0	5.4 6.5	1.4 2.5	6.4 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	4 5	2.5 1.0	5.9 5.5	7.4 7.0	3.4 3.0	8.4 8.0	ns

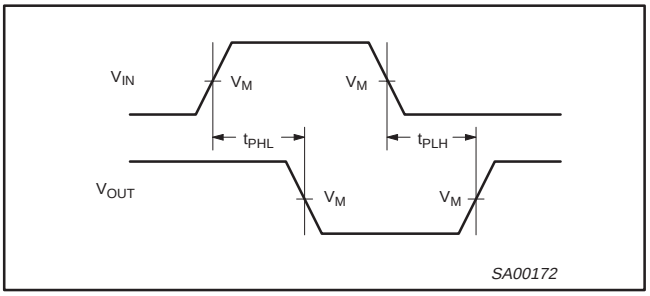
AC SET-UP REQUIREMENTS

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω

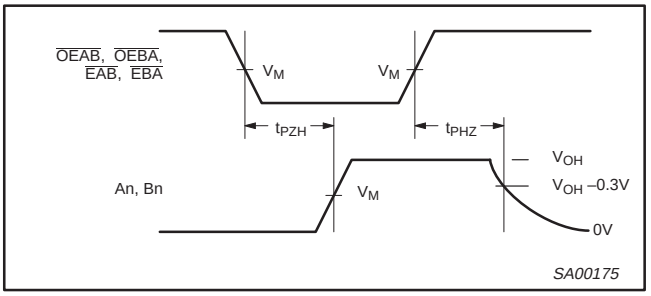
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25 °C, V_{CC} = +5.0 V		T_{amb} = –40 °C to +85 °C, V_{CC} = +5.0 V ±0.5 V	
			Min	Typ	Min	
t_s(H) t_s(L)	Set-up time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	3	3.0 3.0	1.5 0.6	3.0 3.0	ns
t_h(H) t_h(L)	Hold time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	3	0.5 0.5	–0.3 –1.3	0.5 0.5	ns
t_s(H) t_s(L)	Set-up time An to $\overline{EAB}$, Bn to $\overline{EBA}$	3	3.0 3.0	1.5 0.6	3.0 3.0	ns
t_h(H) t_h(L)	Hold time An to $\overline{EAB}$, Bn to $\overline{EBA}$	3	0.5 0.5	–0.2 –1.3	0.5 0.5	ns
t_w(L)	Latch Enable pulse width, LOW	3	3.5	1.8	3.5	ns

AC WAVEFORMS

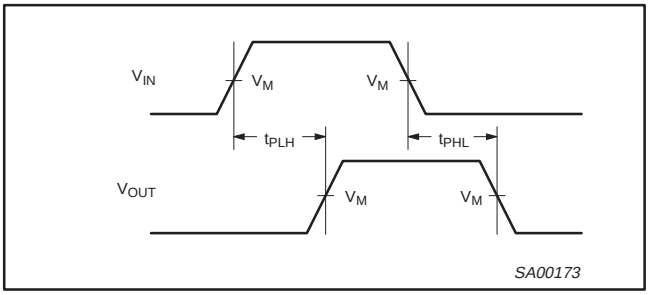
V_M = 1.5 V; V_{IN} = GND to 3.0 V



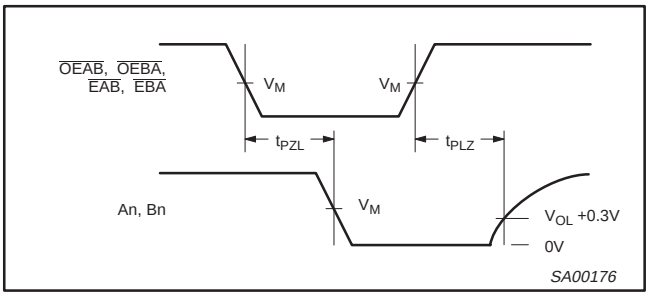
Waveform 1. Propagation delay for inverting output



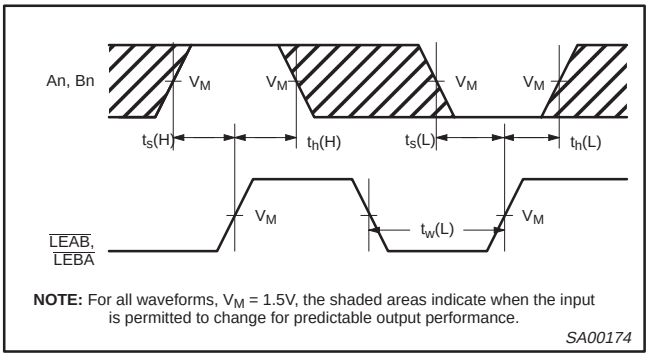
Waveform 4. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level



Waveform 2. Propagation delay for non-inverting output

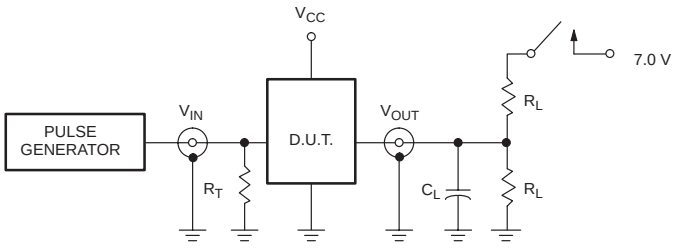


Waveform 5. 3-State Output Enable time to LOW level and Output Disable time from LOW level

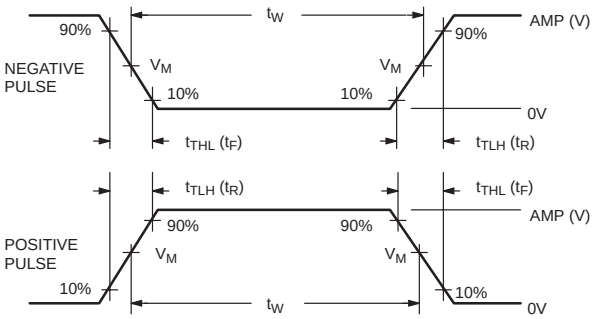


Waveform 3. Data set-up and hold times and Latch Enable pulse width

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5 V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

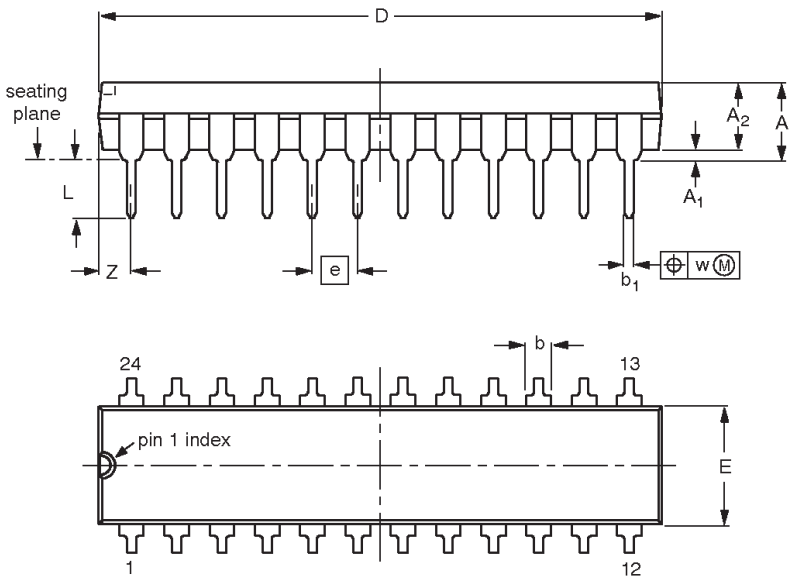
R_L = Load resistor; see AC CHARACTERISTICS for value.

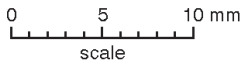
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0 V	1 MHz	500 ns	2.5 ns	2.5 ns

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

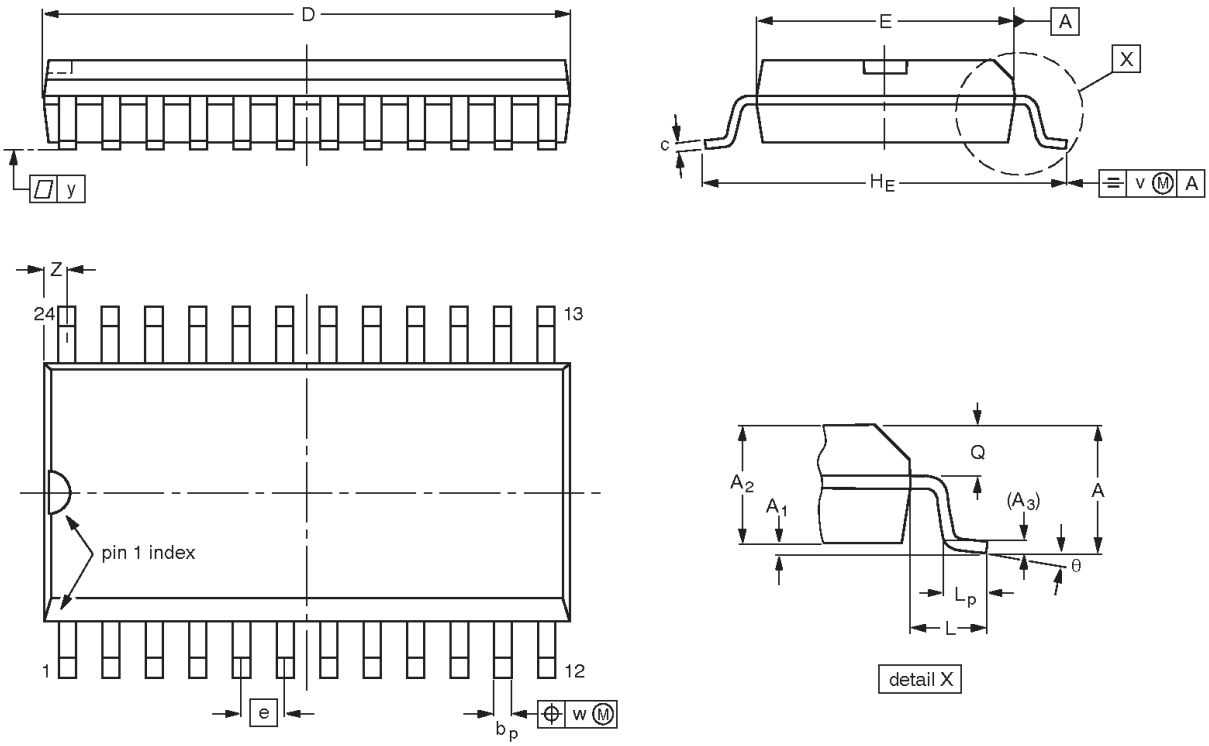
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001				~~99-04-28~~ 99-12-27

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

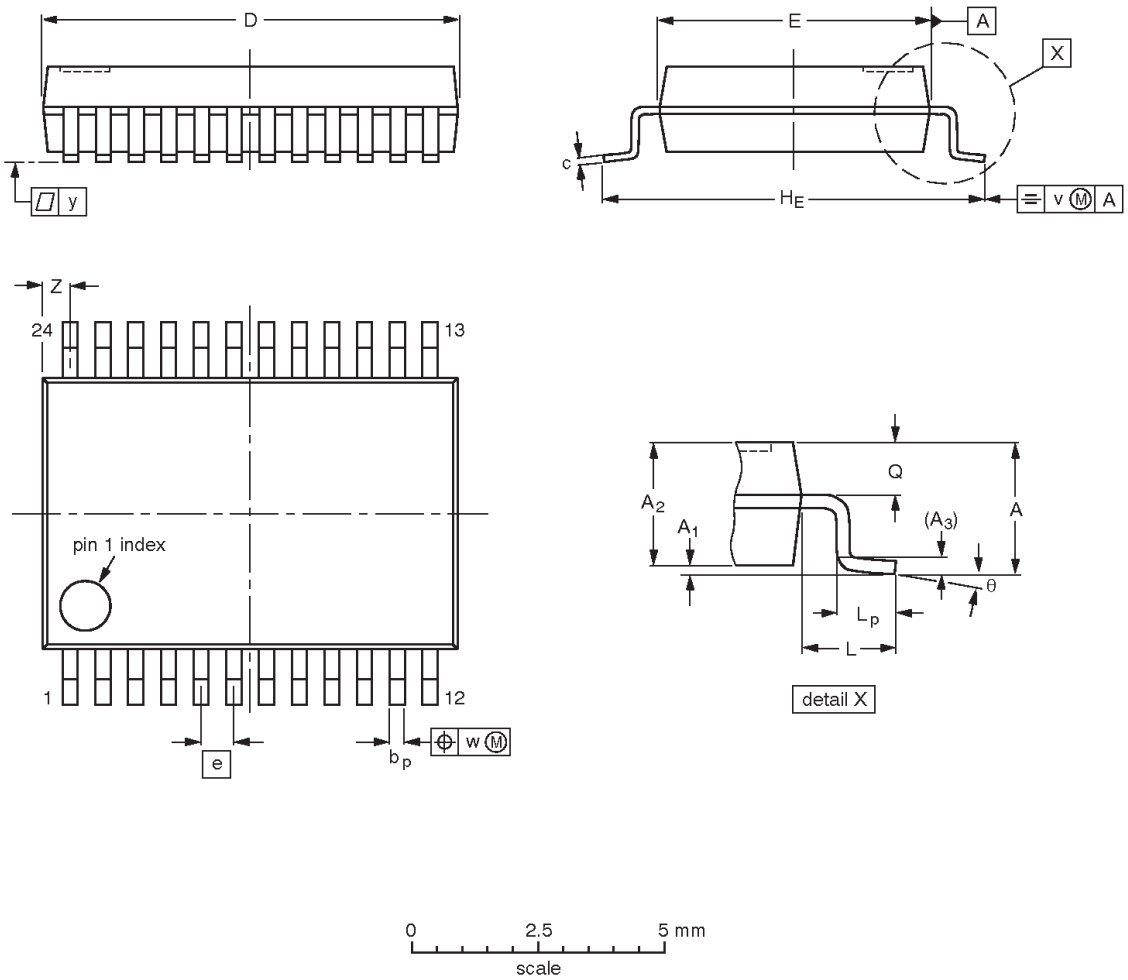
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013				~~97-05-22~~ 99-12-27

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

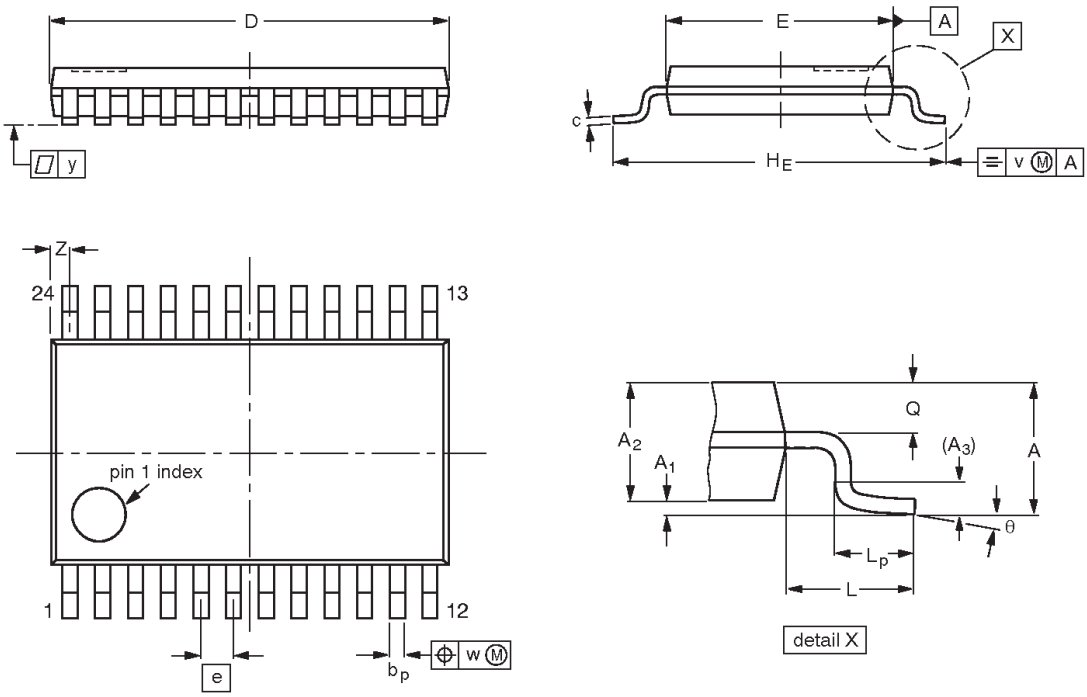
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

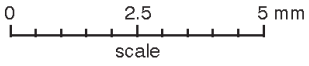
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150				~~95-02-04~~ 99-12-27

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~95-02-04~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_2	20021118	**Product data; second version (9397 750 10752). Supersedes data of 1993 Jun 01.** Engineering Change Notice 853–1610 29205 (date: 20021115).
	19930601	**Product data; initial version.** Engineering Change Notice 853–1610 09907 (date: 19930601).

Octal latched transceiver with dual enable, inverting (3-State)

74ABT544

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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